IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array in which ~~one~~ a block ~~for writing/erasing~~ configured to perform a write/erase operation by a page unit comprises pages; and

a control circuit ~~which manages~~ configured to manage, for each page, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages.

Claim 2 (Currently Amended): The nonvolatile semiconductor memory according to claim 1, wherein the nonvolatile semiconductor memory ~~has~~ is configured to perform a page erase ~~function~~ operation.

Claim 3 (Currently Amended): The nonvolatile semiconductor memory according to claim 1, wherein the control circuit is mounted in the nonvolatile semiconductor memory ~~in a mixed manner~~ on one chip.

Claim 4 (Original): The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in a redundancy area of the memory cell array in the nonvolatile semiconductor memory.

Claim 5 (Original): The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in a special memory cell area different from the memory cell array in the nonvolatile semiconductor memory.

Claim 6 (Original): The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in another nonvolatile semiconductor memory different from the nonvolatile semiconductor memory.

Claim 7 (Currently Amended): The nonvolatile semiconductor memory according to claim 1, wherein the control circuit ~~reads~~ is configured to read the information with respect to all the pages every time data is written/erased.

Claim 8 (Original): The nonvolatile semiconductor memory according to claim 7, wherein the control circuit renewsthe information with respect to the page which is an object of the data write/erase a every time data is written/erased.

Claim 9 (Original): The nonvolatile semiconductor memory according to claim 8, wherein the data write/erase is performed by reading the information, subsequently erasing the data of the page which is the object of data write/erase, and writing renewed data in the page which is the object of data write/erase.

Claim 10 (Currently Amended): The nonvolatile semiconductor memory according to claim 8, wherein the control circuit ~~determines~~ is configured to determine whether ~~or not~~ to perform a refresh ~~for returning~~ to return states of memory cells of all the pages in the block or the page which is the object of data write/erase to initial states based on the information on all the pages every time the data is written/erased.

Claim 11 (Currently Amended): The nonvolatile semiconductor memory according to claim 10, wherein the renew of the information is performed by setting the information ~~on~~

of the page which is the object of data write/erase to the number of data write/erase times of the page which is the object of data write/erase.

Claim 12 (Original): The nonvolatile semiconductor memory according to claim 11, wherein the refresh is executed, when a total value of the number of data write/erase times reaches an allowable value with respect to all the pages.

Claim 13 (Original): The nonvolatile semiconductor memory according to claim 12, wherein the information is initialized by the refresh.

Claim 14 (Original): The nonvolatile semiconductor memory according to claim 10, wherein the renew of the information is performed by setting the information on the page which is the object of data write/erase to a total value of the number of data write/erase times in the block.

Claim 15 (Original): The nonvolatile semiconductor memory according to claim 14, wherein the refresh is executed, when a maximum value of the number of data write/erase times reaches an allowable value with respect to all the pages.

Claim 16 (Original): The nonvolatile semiconductor memory according to claim 15, wherein the information is initialized by the refresh.

Claim 17 (Original): The nonvolatile semiconductor memory according to claim 14, wherein the refresh is executed, when a value obtained by subtracting a minimum value from

a maximum value of the number of data write/erase times reaches an allowable value with respect to all the pages.

Claim 18 (Original): The nonvolatile semiconductor memory according to claim 17, wherein the information is initialized by the refresh.

Claim 19 (Original): The nonvolatile semiconductor memory according to claim 17, wherein the information on the page which is an object of the refresh is renewed by the refresh.

Claim 20 (Original): The nonvolatile semiconductor memory according to claim 10, wherein the data write/erase is performed as a part of the refresh.

Claim 21 (Currently Amended): The nonvolatile semiconductor memory according to claim 1, wherein the nonvolatile semiconductor memory ~~is~~ comprises a NAND-type flash memory.

Claim 22 (Currently Amended): A memory system comprising:

a memory cell array in which ~~one~~ a block ~~for performing~~ configured to perform a data write/erase operation by a page unit comprises pages; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page.

Claim 23 (Original): The memory system according to claim 22, wherein the memory system ~~constitutes~~ comprises a memory card.

Claim 24 (Original): The memory system according to claim 22, wherein the memory system comprises an electronic apparatus comprising: a memory card including the nonvolatile semiconductor memory; and the controller.

Claim 25 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array in which ~~one~~ a block ~~for performing~~ configured to perform a data write/erase operation by an area unit comprises areas; and

a control circuit ~~which manages,~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas.

Claim 26 (Original): The nonvolatile semiconductor memory according to claim 25, wherein each of the areas includes pages.

Claim 27 (Currently Amended): A memory system comprising:

a memory cell array in which ~~one~~ a block ~~for performing~~ configured to perform a data write/erase operation by an area unit comprises areas; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas for each area.

Claim 28 (Original): The memory system according to claim 27, wherein each of the areas includes pages.

Claim 29 (Currently Amended): The memory system according to claim 27, wherein the memory system ~~constitutes~~ comprises a memory card.

Claim 30 (Original): The memory system according to claim 27, wherein the memory system comprises an electronic apparatus comprising: a memory card including the nonvolatile semiconductor memory; and the controller.

Claim 31 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second memory areas in which ~~one~~ a block comprises pages; and

a control circuit ~~which manages,~~configured to manage for each page, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages,

wherein the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

Claim 32 (Currently Amended): A memory system comprising:

a memory cell array comprising first and second memory areas in which ~~one~~ a block comprises pages; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page,

wherein the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

Claim 33 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second memory areas in which ~~one~~ a block comprises areas; and

a control circuit ~~which manages~~ configured to manage, for each area, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas,

wherein the area comprises pages, and the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

Claim 34 (Currently Amended): A memory system comprising:

a memory cell array comprising first and second memory areas in which ~~one~~ a block comprises areas; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas for each area,

wherein the area comprises pages, and the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

Claim 35 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second blocks comprising pages; and

a control circuit ~~which manages~~ configured to manage, for each page, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

Claim 36 (Currently Amended): A memory system comprising:

a memory cell array comprising first and second blocks comprising pages;

and a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

Claim 37 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second blocks comprising areas; and

a control circuit ~~which manages~~ configured to manage, for each area, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas,

wherein the area comprises pages, and the information is alternately stored in one of the first and second blocks every time the data is written/erased.

Claim 38 (Currently Amended): A memory system comprising:

a memory cell array comprising first and second blocks comprising areas; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the areas for each area,

wherein the area comprises pages, and the information is alternately stored in one of the first and second blocks every time the data is written/erased.

Claim 39 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array comprising a first block comprising pages; and

a control circuit ~~which manages~~ configured to manage, for each page, information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages,

wherein the information is alternately stored in one of the first block and a second block in another nonvolatile semiconductor memory including the same constitution as that of the nonvolatile semiconductor memory every time the data is written/erased.

Claim 40 (Currently Amended): A memory system comprising:

a first nonvolatile semiconductor memory, which comprises a first block comprising pages, configured to write/erase ~~and which writes/erases~~ data by a page unit;

a second nonvolatile semiconductor memory which comprises a second block comprising pages, configured to write/erase ~~and which writes/erases~~ the data by the page unit; and

a controller ~~which manages~~ configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

Claim 41 (Currently Amended): A memory system comprising:

a nonvolatile semiconductor memory, in which a block comprises pages and in which each of the pages comprises memory cells disposed in a row direction, configured to select a ~~and which has a function of selecting~~ block erase to be performed by a unit of the block and page erase to be performed by a unit of the page; and

a control circuit ~~which issues~~ configured to issue a command ~~for executing~~ to execute the page erase to the nonvolatile semi-conductor memory.

Claim 42 (Currently Amended): The memory system according to claim 41, wherein the page erase ~~is a function of erasing~~ erases unnecessary data in at least one page in data stored in the block.

Claim 43 (Currently Amended): The memory system according to claim 41, wherein the control circuit ~~manages~~ is configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page.

Claim 44 (Currently Amended): The memory system according to claim ~~43~~, 41 wherein the control circuit ~~manages~~ is configured to manage whether ~~or not~~ a value obtained by subtracting a minimum value from a maximum value reaches an allowable value in the information on all the pages.

Claim 45 (Original): The memory system according to claim 41, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

Claim 46 (Currently Amended): A control method of a nonvolatile semi-conductor memory, in which a block comprises pages and in which each of the pages comprises memory cells arranged in a row direction, configured to select a ~~and which has a function of selecting~~ block erase to be performed by a unit of the block and page erase to be performed by a unit of the page, the method comprising:

erasing unnecessary data in at least one page in data stored in the block by the page erase.

Claim 47 (Currently Amended): The control method according to claim 46, ~~wherein the control circuit manages~~ further comprising:

managing information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page.

Claim 48 (Currently Amended): The control method according to claim 46, further comprising:

managing ~~wherein the control circuit manages~~ whether ~~or not~~ a value obtained by subtracting a minimum value from a maximum value reaches an allowable value in the information on all the pages.

Claim 49 (Original): The control method according to claim 46, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

Claim 50 (Currently Amended): A nonvolatile semiconductor memory comprising:

a memory cell array in which a block comprises pages and in which each of the pages comprises memory cells arranged in a row direction;

~~a function of selecting~~ a unit configured to select a block erase to be performed by a unit of the block and a page erase to be performed by a unit of the page; and

~~a function of managing~~ a unit configured to manage information associated with ~~the number~~ respective numbers of data write/erase times ~~with respect to each~~ of the pages for each page.

Claim 51 (Currently Amended): The nonvolatile semiconductor memory according to claim 50, wherein the page erase ~~is a function of erasing~~ erases unnecessary data in at least one page in data stored in the block.

Claim 52 (Original): The nonvolatile semiconductor memory according to claim 50, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

Claim 53 (Original): A memory system comprising: the nonvolatile semiconductor memory according to claim 50.